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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,154	09/23/2002	Yeou-Min Yeh	ALIP0009USA	2781

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,154	YEH, YEOU-MIN	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/23/02; 10/08/02; 10/22/02; 12/15/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *18-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,10 and 15-17* is/are rejected.

7)☒ Claim(s) *4-5, 7-9, 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/08/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Election/Restrictions filed 12/15/2005.

2. Claims 1-51 are pending in this application. Claim 1 is independent claim. In the reply, claims 1-17 are elected and claims 18-51 are withdrawn. This Office action is made non-final.

Election/Restrictions

3. This application contains claims directed to the following patentably distinct species of the claimed invention:

a. Species I: Claims 2-17 are drawn to structure of Butterfly Units I, II, and III for used in FFT/IFFT processor.

b. Species II: Claims 18-51 are drawn to structure of a reordering circuit.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, 1 is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after

the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

2. Applicant's election of Group I (claims 1-17) in the reply filed on 12/15/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Information Disclosure Statement

3. The information disclosure statement filed 10/28/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. There is no copy of reference 5 "Pipeline and Parallel-pipeline FFT Processors for VLSI Implementation".

Claim Objections

4. Claims 6 and 10 are objected to because of the following informalities:

Re claims 6 and 10, the applicant is advised to remove the period "." at the end of line 25 page 4 and line 20 page 6 respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 6, and 10, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Lihong Jia et al. ("Implementation of A Low Power 128-Point FFT").

Re claim 1, Lihong Jia et al. disclose in Figures 1-4 a pipelined N-point transform processor (e.g. Figure 4 and left column page 371) comprising: a first triplet comprising a first butterfly unit (BFI), a butterfly unit (BFII) and a butterfly unit (BFIII) connected together in series (e.g. PE1, PE2, and PE3 respectively in Figure 4), an input port of the first BFI serving as an input port of the triplet to accept complex numbers, an output port of the BFIII serving as an output port of the triplet (e.g. dash-line around the three PE units); a complex multiplier (e.g. multiplier in between PE3 and PE1 in Figure 4) accepting a complex result from the output port of the first triplet (e.g. output of PE3 in the dash-line box), and accepting a coefficient (e.g. W) to generate a complex product (e.g. output or input into the next PE1); an output portion comprising at least a second BFI (e.g. output of PE1), an input port of the second BFI accepting the complex product from the complex multiplier, the output portion providing output transformed complex numbers (e.g. output of PE1); and a control unit (e.g. Control Unit in Figure 4 and left column in page 371) comprising a pipeline step-count register, and means for providing coefficients to the complex multiplier (e.g. right column in page 369) wherein the control

unit controls each BFI, each BFII, each BFIII, and provides each coefficient according to a value held in the pipeline step-count register (e.g. pipeline architecture).

Re claim 2, Lihong Jia et al. further disclose in Figures 1-4 the means for providing coefficients to the complex multiplier includes a table of coefficients stored in the control unit (e.g. right column in page 369).

Re claim 3, Lihong Jia et al. further disclose in Figures 1-4 each BFI comprises: a first first-in-first-out (FIFO) buffer (e.g. all the loopback boxes with label 32, 16, 8, 4, 2, and 1) capable of storing at least a complex number; a first complex adder (e.g. top adder in Figure 2) accepting input from the first FIFO and from the input port of the BFI to generate a resulting first complex sum; a first complex subtractor (e.g. bottom adder in Figure 2) accepting input from the first FIFO and from the input port of the BFI to generate a resulting first complex difference; a first multiplexer as an output port of the BF1, the first multiplexer selecting a value from the first PIFO or the first complex sum from the first complex adder according to a first control line; and a second multiplexer for providing input to the first FIFO, the second multiplexer selecting a value from the input port of the BFI or the first complex difference from the first complex subtractor according to a second control line; wherein the first control line and the second control line are driven by the control unit according to a value held within the pipeline step-count register (e.g. inherently for controlling the PE stage FFT in pipeline manner).

Re claim 6, it is similar to claim 3 wherein the complex signal is rotated by pi/2 (e.g. right column last paragraph in page 369). Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 10, it is similar to claim 3 wherein the complex signal is rotated by pi/2 (e.g. right column last paragraph in page 369 and Figure 3 with multiplication of j/-j). Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 15, Lihong Jia et al. further disclose in Figures 1-4 N=2n, n mod 3 equals 2, and the output portion further comprises a second BFII serially connected to the second BFI (e.g. Figure 4 with the PE2 outside the dash-line).

Re claim 16, Lihong Jia et al. further disclose in Figures 1-4 $N=2^n$, n mod 3 equals 0, and the output portion further comprises a second BFII serially connected to the second BFI, and a second BFIII serially connected to the second BFII (e.g. Figure 4 with PE3 connected outside the dash-line).

Re claim 17, Lihong Jia et al. further disclose in Figures 1-4 the transform processor is an N-point Decimation in Time Inverse Fast Fourier Transform (DIT IFFT) processor (e.g. Figure 3 in page 370).

Allowable Subject Matter

6. Claims 4-5, 7-9, and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,821,224 to Liu et al. disclose a method and apparatus for processing multi-dimensional data to obtain a fourier transform.

b. U.S. Patent No. 6,658,441 to Kim discloses an apparatus and method for recursive parallel and pipelined fast fourier transform.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

February 16, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100